FIG. 1A PRIOR ART

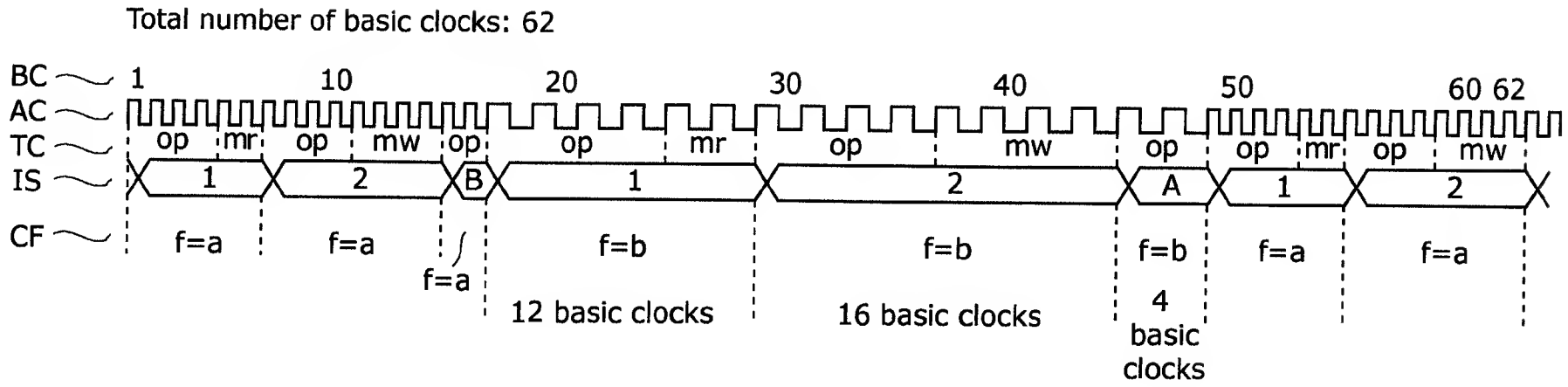


FIG. 1B

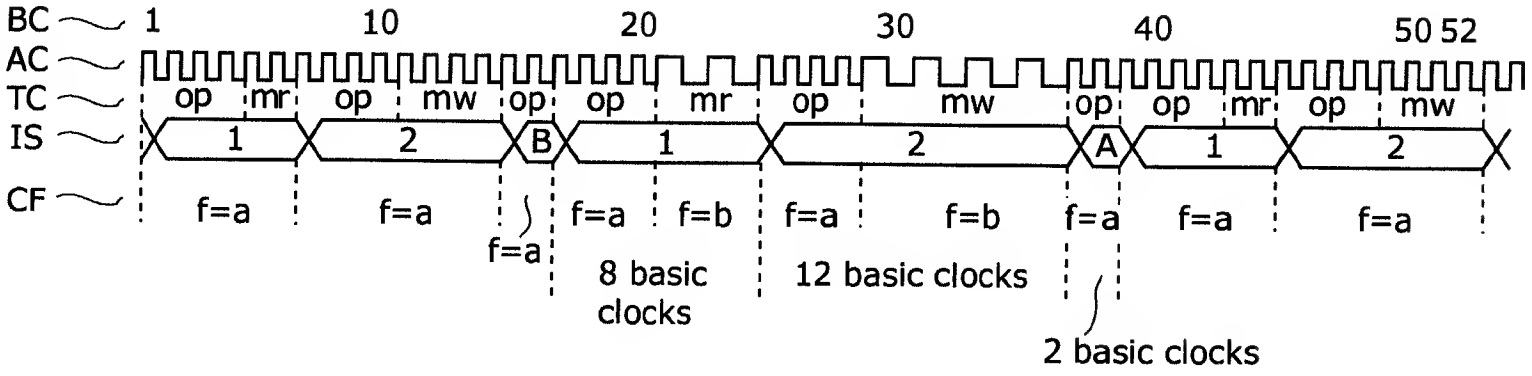


FIG. 2

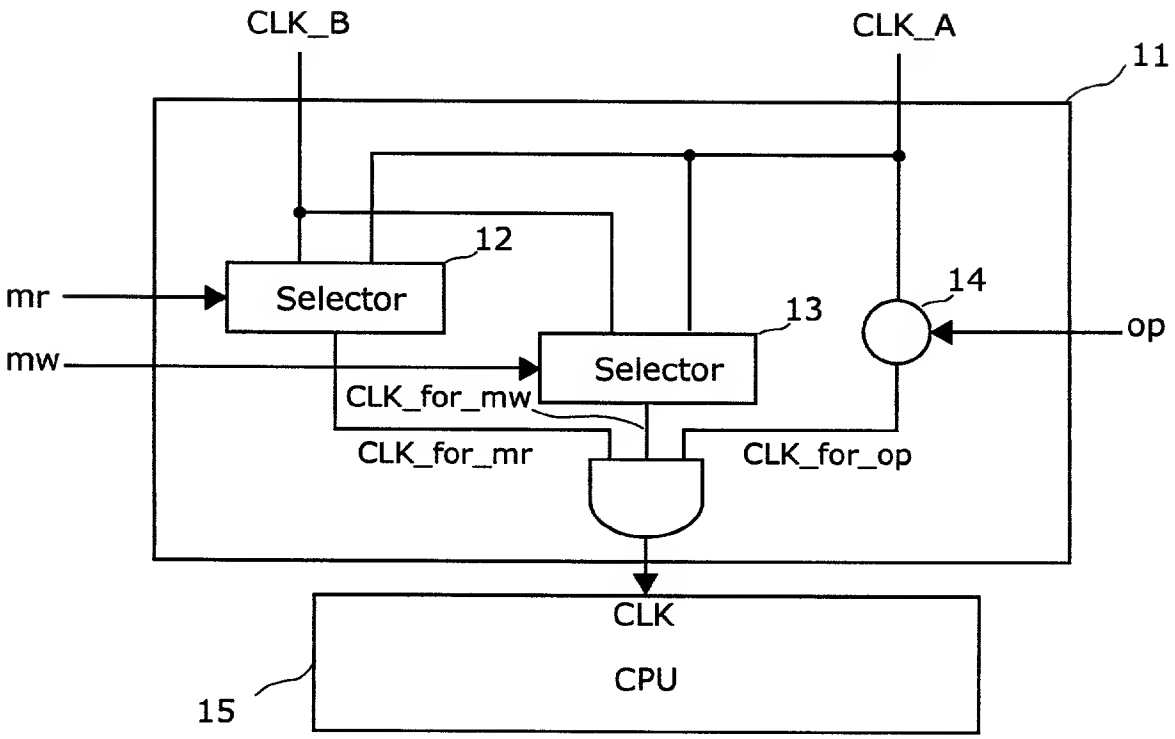

CLK_B
CLK_A
11
12
mr
Selector
14
13
op
mw
Selector
CLK_for_mw
CLK_for_mr
CLK_for_op
CLK
CPU
15

FIG. 3A

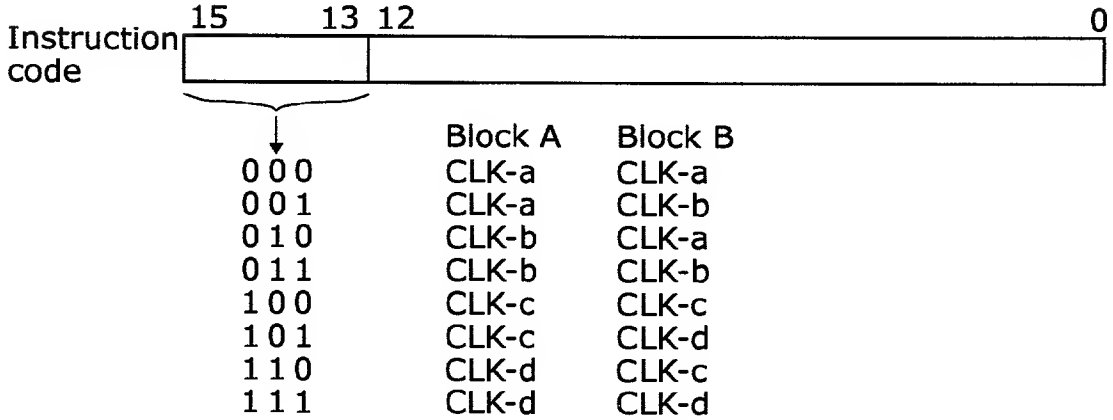

Instruction code
15
13
12
0
Block A
Block B
000 CLK-a CLK-a
001 CLK-a CLK-b
010 CLK-b CLK-a
011 CLK-b CLK-b
100 CLK-c CLK-c
101 CLK-c CLK-d
110 CLK-d CLK-c
111 CLK-d CLK-d

FIG. 3B

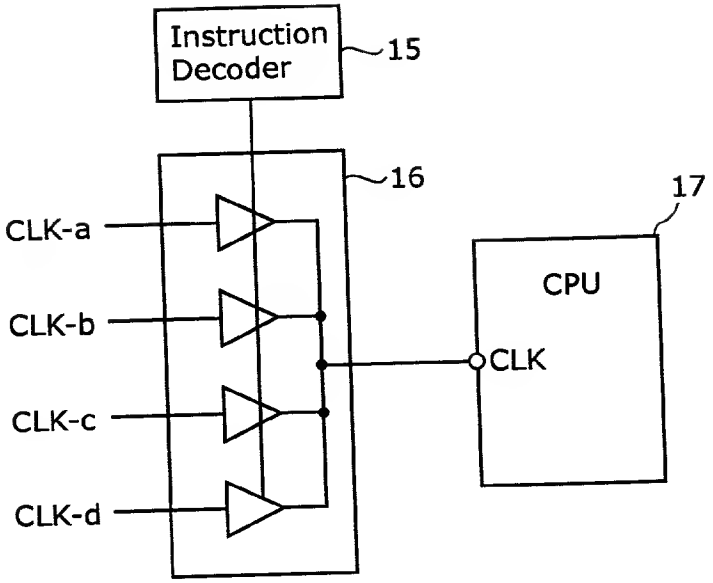

Instruction Decoder
15
16
17
CLK-a
CLK-b
CLK-c
CLK-d
CPU
CLK

FIG. 3C

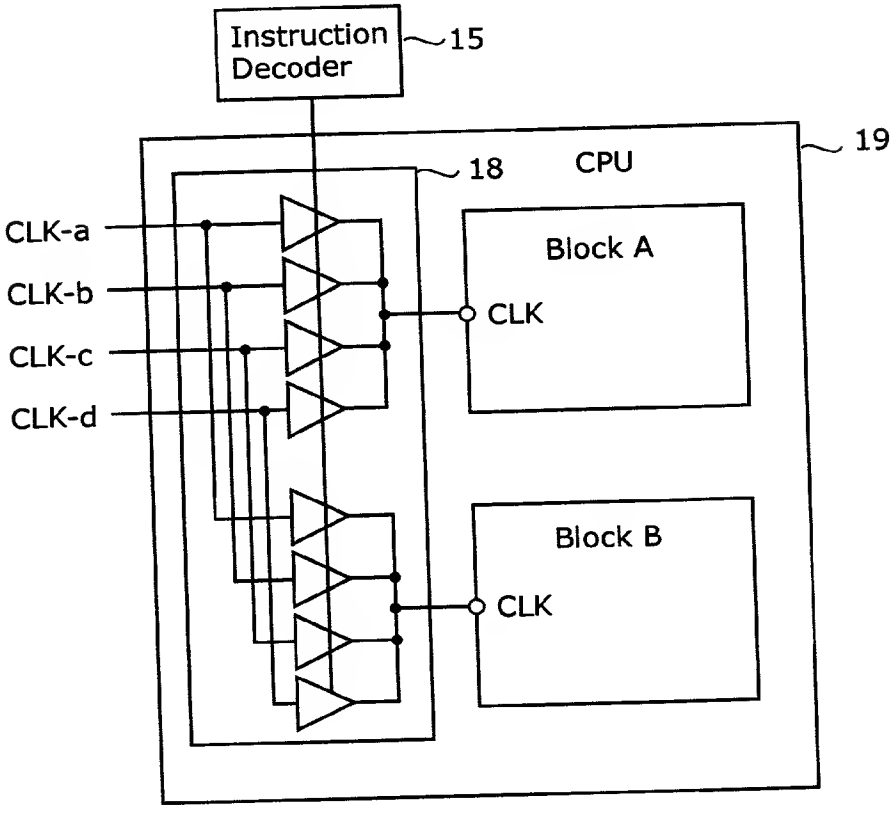

Instruction Decoder
15
19
18
CPU
CLK-a
CLK-b
CLK-c
CLK-d
Block A
CLK
Block B
CLK

FIG. 4A

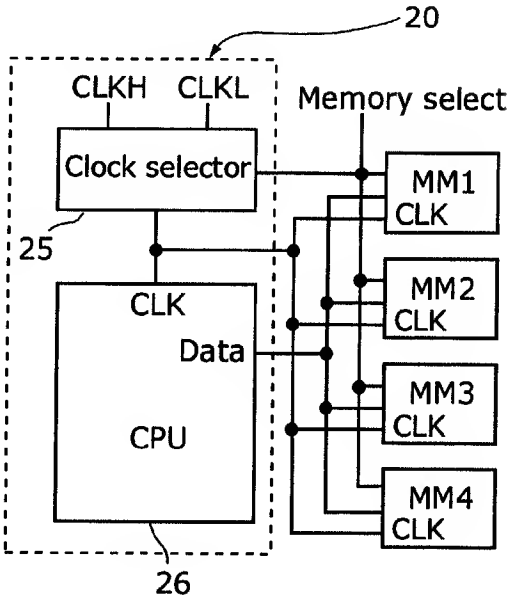


FIG. 4B

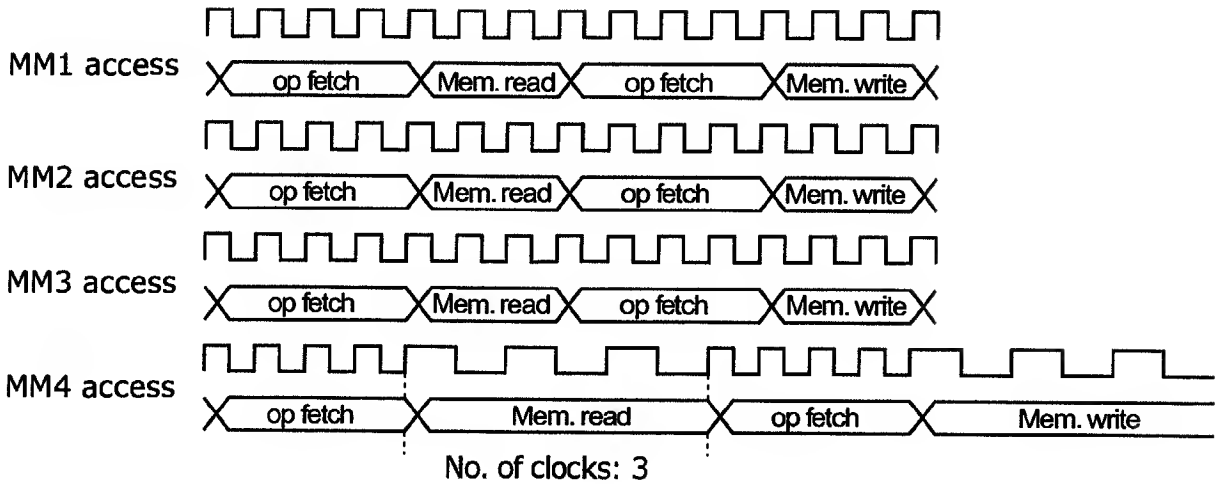


FIG. 4C PRIOR ART

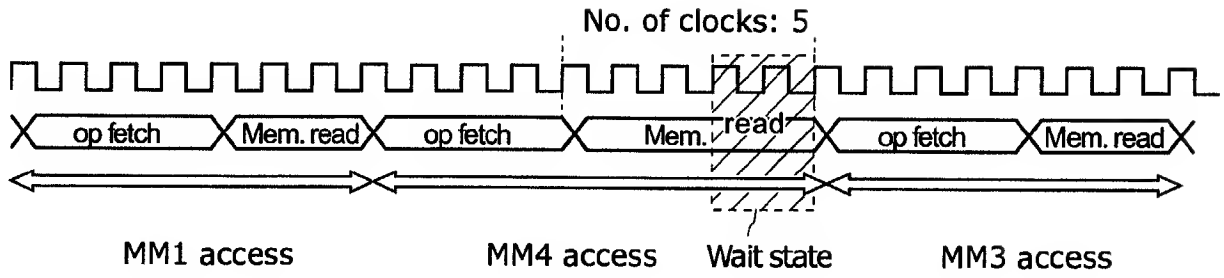


FIG. 5

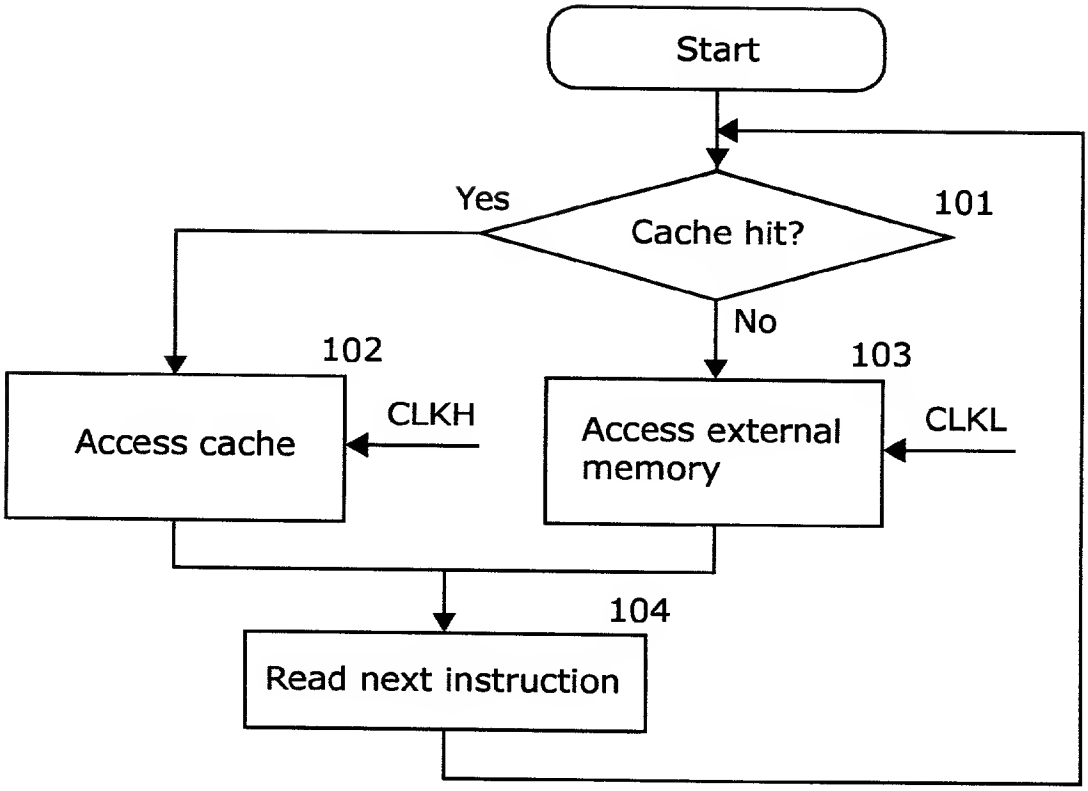
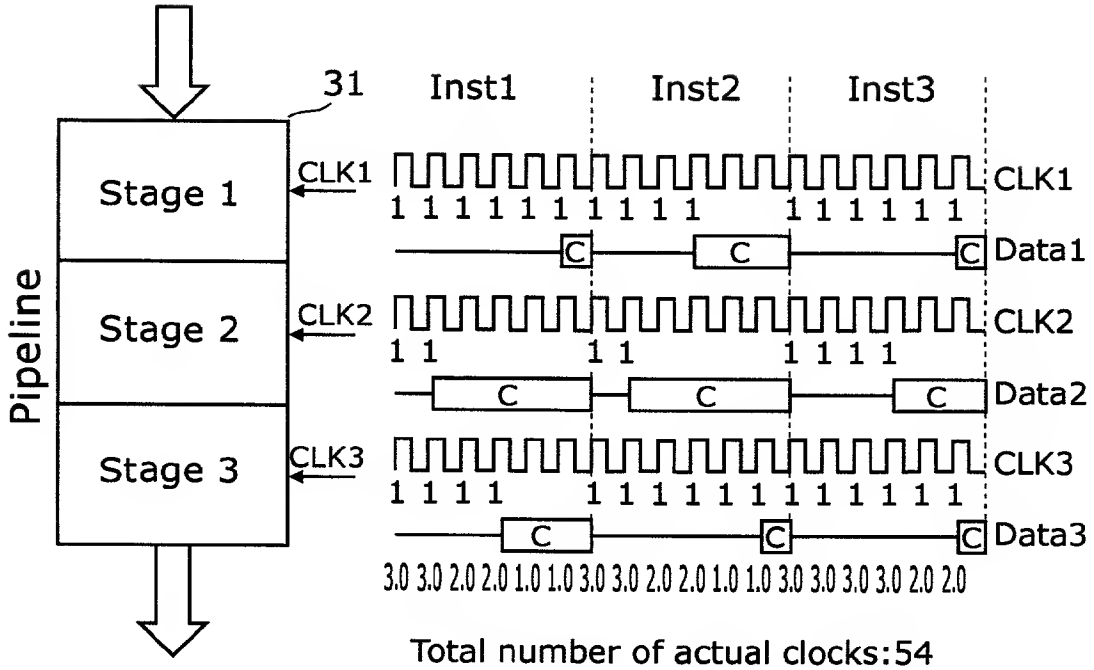
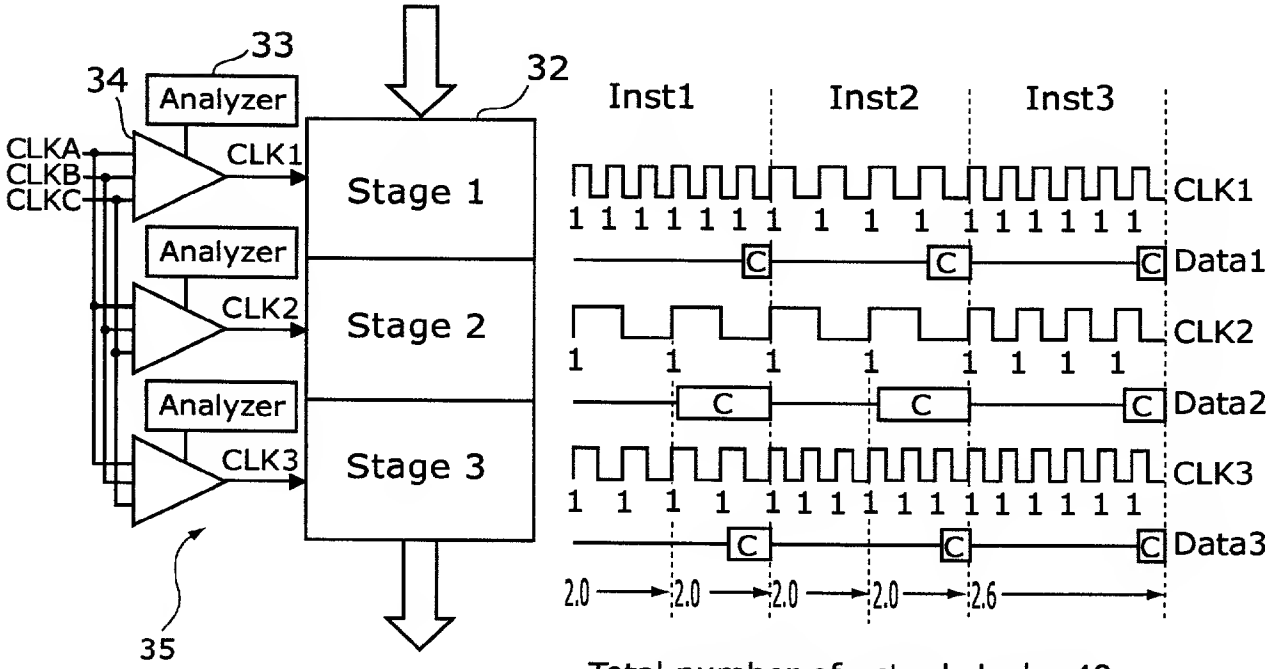

Start
Cache hit?
101
Yes
No
102
103
Access cache
CLKH
Access external memory
CLKL
104
Read next instruction

FIG. 6A PRIOR ART



Total number of actual clocks:54

FIG. 6B



Total number of actual clocks:40

FIG. 7A

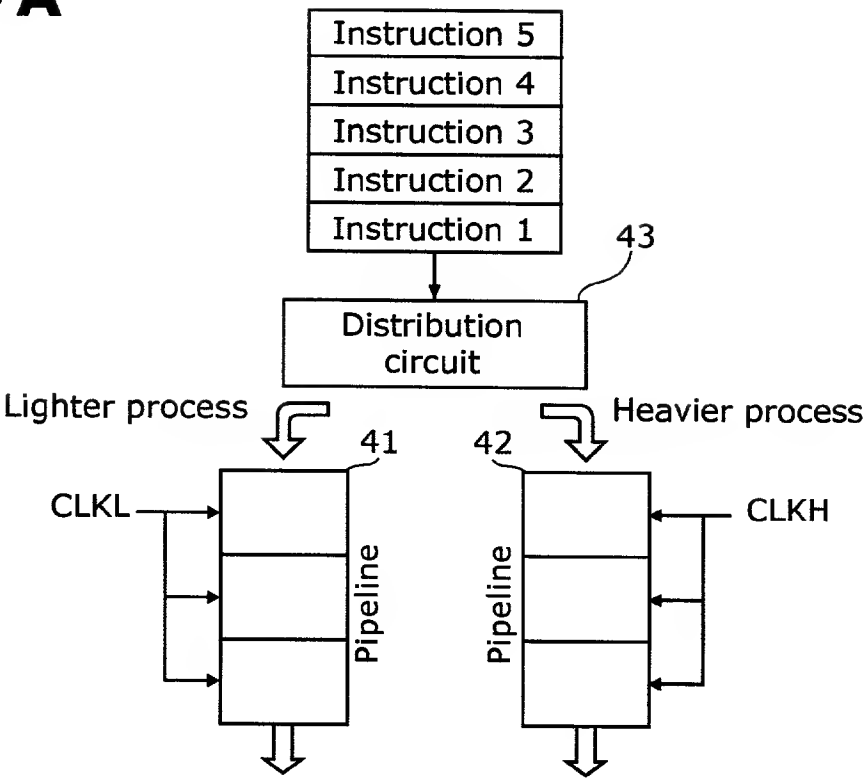


FIG. 7B

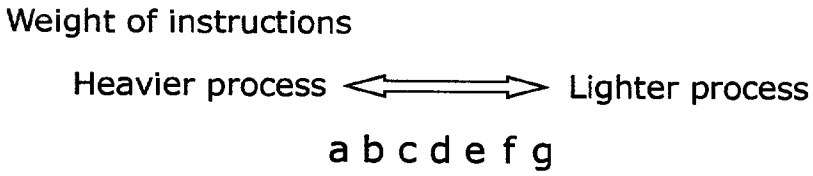


FIG. 7C

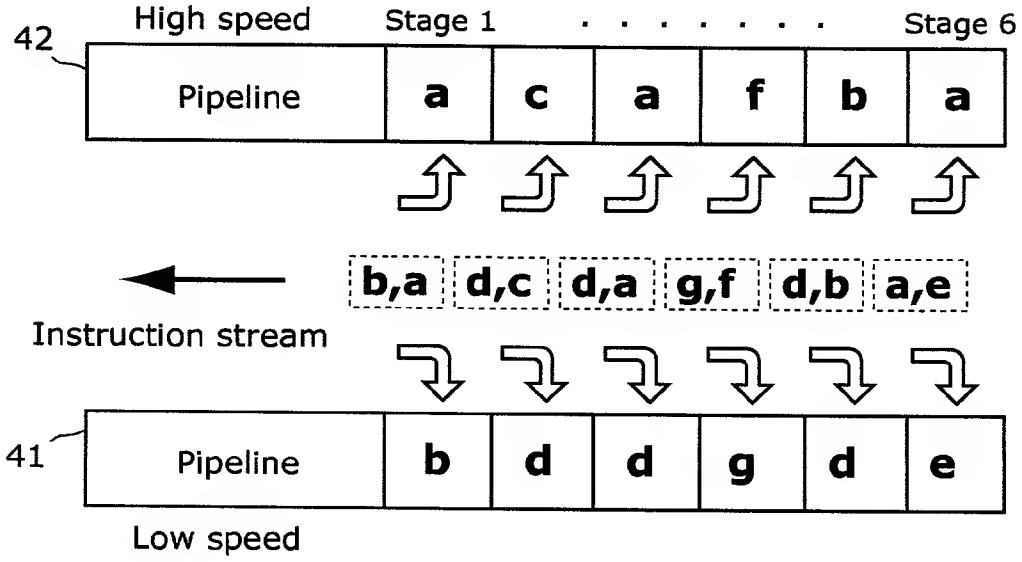


FIG. 8

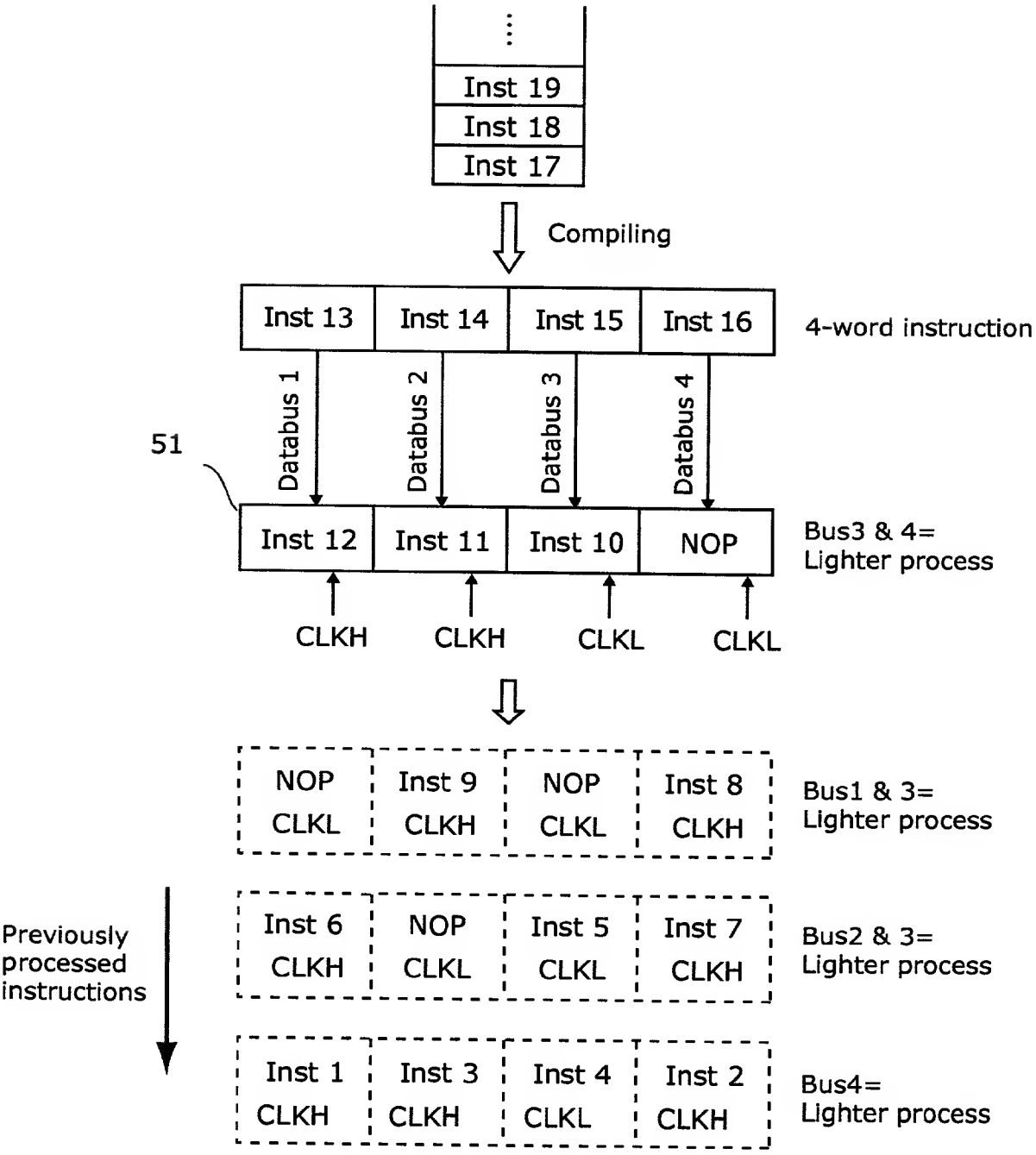

Inst 19
Inst 18
Inst 17
Compiling
Inst 13
Inst 14
Inst 15
Inst 16
4-word instruction
Databus 1
Databus 2
Databus 3
Databus 4
51
Inst 12
Inst 11
Inst 10
NOP
Bus3 & 4=
Lighter process
CLKH
CLKH
CLKL
CLKL
NOP
CLKL
Inst 9
CLKH
NOP
CLKL
Inst 8
CLKH
Bus1 & 3=
Lighter process
Previously
processed
instructions
Inst 6
CLKH
NOP
CLKL
Inst 5
CLKL
Inst 7
CLKH
Bus2 & 3=
Lighter process
Inst 1
CLKH
Inst 3
CLKH
Inst 4
CLKL
Inst 2
CLKH
Bus4=
Lighter process

FIG. 9A PRIOR ART

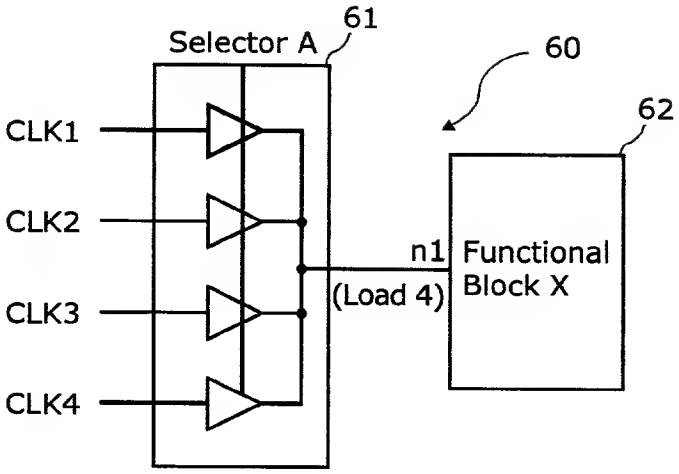


FIG. 9B

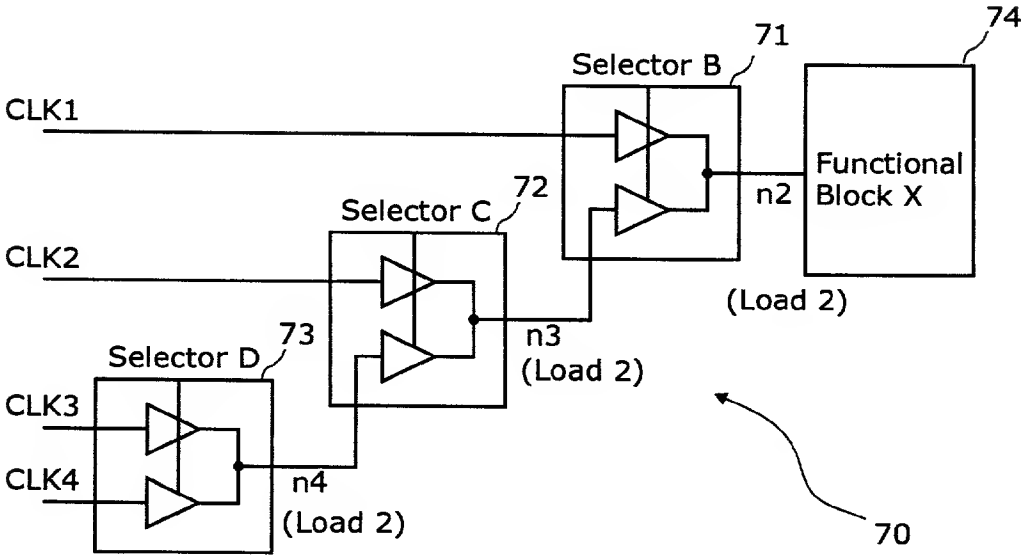


FIG. 9C

CLK Transition	CLK1	CLK2	CLK1	CLK2	CLK3
Clock selector block 60	4	4	4	4	4
Clock selector block 70	2	2	2	2	4

FIG. 10

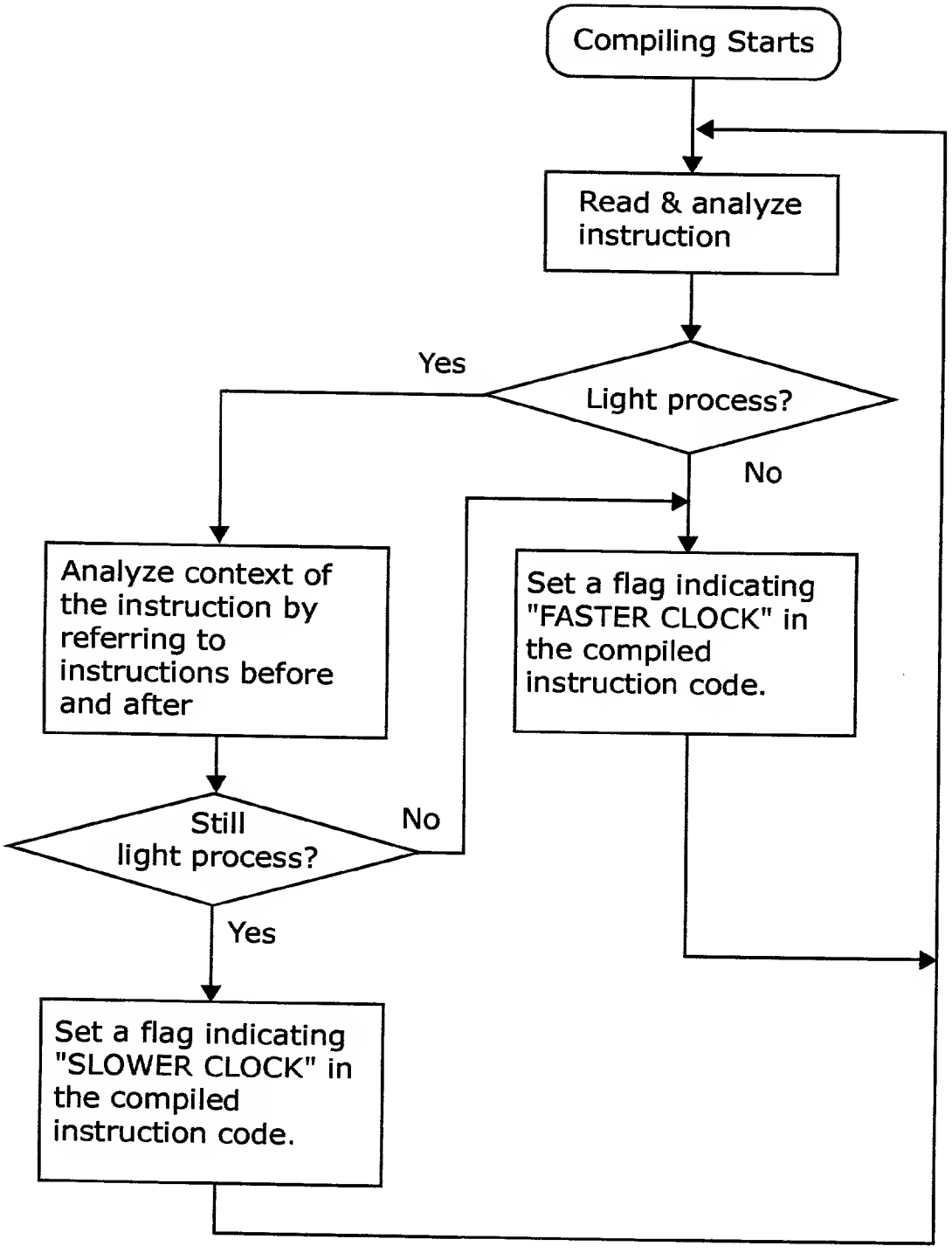

Compiling Starts
Read & analyze instruction
Light process?
Yes
No
Analyze context of the instruction by referring to instructions before and after
Still light process?
No
Yes
Set a flag indicating "SLOWER CLOCK" in the compiled instruction code.
Set a flag indicating "FASTER CLOCK" in the compiled instruction code.

FIG. 11A PRIOR ART

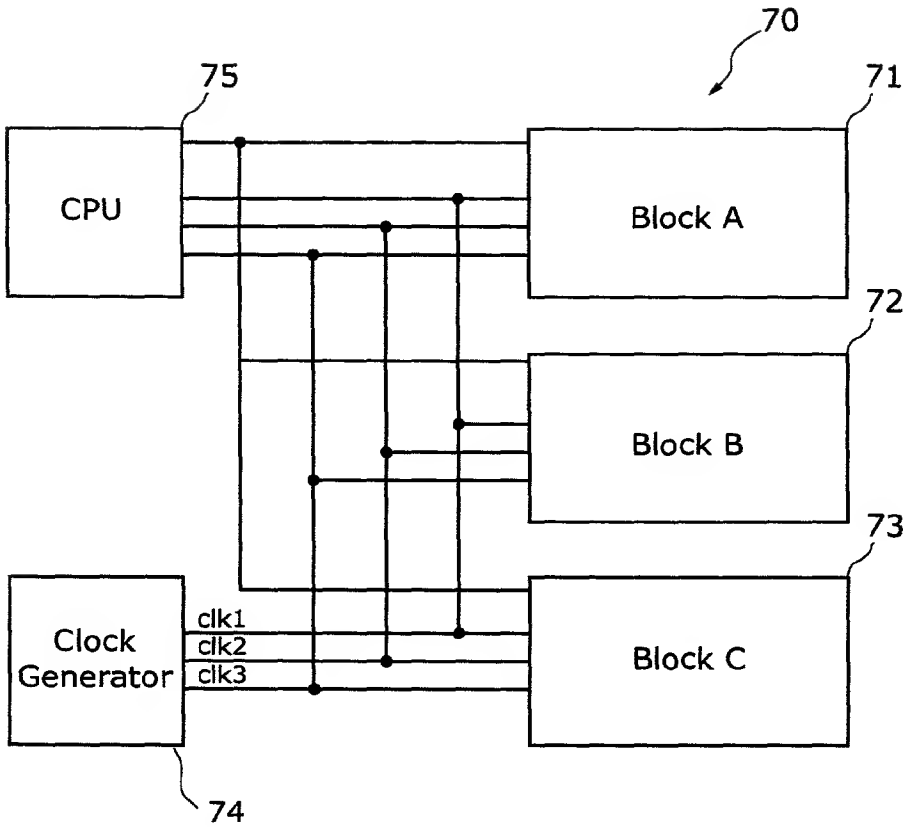


FIG. 11B PRIOR ART

Cycle	Block A	Block B	Block C
1	V		
2		V	
3	V		B
4	O	O	O
5		B	

V: Very active operation
O: Ordinally operation
B: Barely noticeable operation